

1 CLAIMS

2 *claim 1* 1. An integrated circuit, comprising:
3 one or more components that receive a distributed voltage;
4 a voltage driver that produces a compensated voltage, the compensated
5 voltage being distributed to form the distributed voltage at the one or more
6 components, wherein the distributed voltage is degraded relative to the
7 compensated voltage; and

8 wherein the voltage driver is responsive to feedback derived from the
9 distributed voltage to adjust the compensated voltage so that the distributed
10 voltage is approximately equal to a nominal voltage.

11
12 2. An integrated circuit as recited in claim 1, wherein said one or more
13 components have input characteristics that contribute to the degradation of the
14 distributed voltage.

15
16 3. An integrated circuit as recited in claim 1, wherein said distribution
17 contributes to the degradation of the distributed voltage.

18
19 4. An integrated circuit as recited in claim 1, wherein:
20 said distribution contributes to the degradation of the distributed voltage;
21 and
22 the compensated voltage is distributed over impedance-matched conductors
23 to form the distributed voltage at the one or more components.
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1 5. An integrated circuit as recited in claim 1, wherein said one or more
2 components comprise data receivers that evaluate data signals relative to the
3 distributed voltage.

4
5 6. An integrated circuit as recited in claim 1, further comprising a
6 feedback component that evaluates the distributed voltage relative to the nominal
7 voltage to derive said feedback.

8
9 7. An integrated circuit as recited in claim 1, wherein:
10 said one or more components have input characteristics that contribute to
11 the degradation of the distributed voltage at the data receivers;
12 further comprising a feedback component that evaluates the distributed
13 voltage relative to the nominal voltage to derive said feedback, wherein the
14 feedback receiver has input characteristics similar to those of the one or more
15 components to contribute similar degradation to the distributed voltage at the
16 feedback component.

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18 8. An integrated circuit as recited in claim 1, wherein:
19 the integrated circuit further comprises a feedback component that
20 evaluates the distributed voltage relative to the nominal voltage to derive said
21 feedback;
22 said distribution contributes to the degradation of the distributed voltage;
23 and
24 the distributed voltage is routed to result in similar degradations at the one
25 or more components and the feedback component.

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9. An integrated circuit as recited in claim 1, further comprising:
a feedback component that evaluates the distributed voltage relative to the nominal voltage to derive said feedback;
wherein the voltage driver has a variable gain that is configured to increase in response to the feedback when the distributed voltage is less than the nominal voltage and to decrease in response to the feedback when the distributed voltage is greater than the nominal voltage.
10. An integrated circuit as recited in claim 1, wherein the voltage driver has a variable gain that is controlled by a digital value.
11. An integrated circuit as recited in claim 1, wherein the voltage driver has a variable gain that is controlled by a digital value, the integrated circuit further comprising a register that is configurable to store the digital value and to provide the digital value to the voltage driver.
12. An integrated circuit as recited in claim 1, wherein the voltage driver has a variable gain that is controlled by a digital value, the integrated circuit further comprising a register that is configurable to store the digital value and to provide the digital value to the voltage driver, the register being readable and writable.

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13. An integrated circuit as recited in claim 1, wherein the voltage driver has a variable gain that is controlled by a digital value, further comprising a counter that produces the digital value, wherein the counter is responsive to the feedback to increment and decrement the digital value.

14. An integrated circuit as recited in claim 1, wherein the voltage driver has a variable gain that is controlled by a digital value, further comprising a counter that produces the digital value, wherein the counter is responsive to the feedback during an initialization period to increment and decrement the digital value, the digital value remaining constant during an operational period following the initialization period.

15. An integrated circuit as recited in claim 1, wherein the integrated circuit comprises a memory device.

16. An integrated circuit as recited in claim 1, wherein the integrated circuit is a memory device that further comprises a plurality of memory storage cells.

17. An integrated circuit, comprising:
a one or more data receivers that evaluate one or more corresponding data signals relative to a distributed reference voltage;
a reference voltage driver that produces a compensated reference voltage, the compensated reference voltage being distributed to form the distributed

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1 reference voltage, wherein the distributed reference voltage is degraded relative to
2 the compensated reference voltage; and

3 wherein the reference voltage driver has a variable gain that increases when
4 the distributed reference voltage is less than a nominal reference voltage and
5 decreases when the distributed reference voltage is greater than the nominal
6 reference voltage.

7
8 **18.** An integrated circuit as recited in claim 17, wherein the reference
9 voltage driver is configured so that its gain is set during an initialization period
10 and remains constant during a subsequent operational period.

11
12 **19.** An integrated circuit as recited in claim 17, wherein the variable
13 gain is controlled by a digital value.

14
15 **20.** An integrated circuit as recited in claim 1, wherein the variable gain
16 is controlled by a digital value, the integrated circuit further comprising a register
17 that is configurable to store the digital value and to provide the digital value to the
18 reference voltage driver.

19
20 **21.** An integrated circuit as recited in claim 1, wherein the variable gain
21 is controlled by a digital value, the integrated circuit further comprising a register
22 that is configurable to store the digital value and to provide the digital value to the
23 reference voltage driver, the register being readable and writable.

1 **22.** An integrated circuit as recited in claim 17, wherein the variable
2 gain is controlled by a digital value, further comprising a counter that produces the
3 digital value, wherein the counter increments or decrements the digital value
4 depending on the relationship of the distributed reference voltage relative to the
5 nominal reference voltage.

6
7 **23.** An integrated circuit as recited in claim 17, wherein the variable
8 gain is controlled by a digital value, and the integrated circuit further comprises a
9 counter that produces the digital value, wherein the counter is configured to
10 increase and decrease the digital value during an initialization period depending on
11 the relationship of the distributed reference voltage and the nominal reference
12 voltage, the digital value remaining constant during an operational period
13 following the initialization period.

14
15 **24.** An integrated circuit as recited in claim 17, further comprising a
16 capacitive charge pump that controls the gain of the reference voltage driver.

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18 **25.** An integrated circuit as recited in claim 17, further comprising a
19 feedback component that evaluates the distributed reference voltage relative to the
20 nominal reference voltage to generate a feedback signal, the reference voltage
21 driver being response to the feedback signal to increase and decrease the variable
22 gain.

1 **26.** An integrated circuit as recited in claim 17, further comprising:
2 a feedback component that evaluates the distributed reference voltage
3 relative to the nominal reference voltage to generate a feedback signal;
4 a charge pump that produces a control voltage to establish the gain of the
5 reference voltage driver;
6 the charge pump being responsive to the feedback signal to increase and
7 decrease the variable gain.

8
9 **27.** An integrated circuit as recited in claim 17, wherein the
10 compensated reference voltage is distributed over impedance-matched conductors
11 to form the distributed reference voltage at the one or more data receivers.

12
13 **28.** An integrated circuit as recited in claim 17, further comprising:
14 a feedback component that evaluates the distributed reference voltage
15 relative to the nominal reference voltage to generate a feedback signal, the
16 reference voltage driver being responsive to the feedback signal to increase and
17 decrease the variable gain;
18 wherein the feedback component incorporates a low-pass filter.

19
20 **29.** An integrated circuit as recited in claim 17, wherein the one or more
21 data receivers comprise a plurality of the data receivers, and wherein the data
22 receivers have similar input characteristics and the distributed reference voltage is
23 routed similarly to each of the data receivers to result in similar degradation of the
24 distributed reference voltage at each of the data receivers.
25

1 **30.** An integrated circuit as recited in claim 17, further comprising:
2 a feedback receiver that evaluates the distributed reference voltage relative
3 to the nominal reference voltage to generate a feedback signal, the reference
4 voltage driver being response to the feedback signal to increase and decrease the
5 variable gain;

6 wherein the data and feedback receivers have similar input characteristics
7 and the distributed reference voltage is routed similarly to the data and feedback
8 receivers to result in similar degradation of the distributed reference voltage at the
9 data and feedback receivers.

11 **31.** An integrated circuit as recited in claim 17, further comprising:
12 a feedback receiver that evaluates the distributed reference voltage relative
13 to the nominal reference voltage to generate a feedback signal, the reference
14 voltage driver being response to the feedback signal to increase and decrease the
15 variable gain;

16 wherein the data and feedback receivers have similar input characteristics
17 and the distributed reference voltage is routed similarly to the data and feedback
18 receivers to result in similar degradation of the distributed reference voltage at the
19 data and feedback receivers; and

20 wherein the feedback receiver incorporates a low-pass filter that does not
21 significantly affect the input characteristics of the feedback receiver.

1 32. An integrated circuit as recited in claim 17, wherein the integrated
2 circuit is a memory device that further comprises a plurality of memory storage
3 cells.

4
5 33. An integrated circuit, comprising:
6 a plurality of data receivers that evaluate corresponding data signals relative
7 to a distributed reference voltage;

8 a feedback receiver that evaluates the distributed reference voltage relative
9 to a nominal reference voltage to produce a feedback signal;

10 a reference voltage driver that produces a compensated reference voltage,
11 the compensated reference voltage being routed on the integrated circuit to form
12 the distributed reference voltage at the data and feedback receivers, wherein the
13 input characteristics of the data and feedback receivers cause a voltage change in
14 the distributed reference voltage at each receiver relative to the compensated
15 reference voltage;

16 the data and feedback receivers having similar input characteristics so that
17 said relative voltage change in the distributed reference voltage is approximately
18 the same at each of the data and feedback receivers;

19 an increment/decrement component that produces a digital value in
20 response to the feedback signal, the increment/decrement component being
21 configured to increment and decrement the digital value depending on the
22 relationship of the distributed reference voltage and the nominal reference voltage
23 as indicated by the feedback signal; and

24 wherein the reference voltage driver has a variable gain that is established
25 by the digital value.

1
2 **34.** An integrated circuit as recited in claim 33, wherein the
3 compensated reference voltage is distributed over impedance-matched conductors
4 to form the distributed reference voltage at the data and feedback receivers.
5

6 **35.** An integrated circuit as recited in claim 33, wherein the
7 increment/decrement component is enabled during an initialization period and the
8 digital value remains constant during a subsequent operational period.
9

10 **36.** An integrated circuit as recited in claim 33, further comprising a
11 register that is configurable to store the digital value and to provide the digital
12 value to the reference voltage driver.
13

14 **37.** An integrated circuit as recited in claim 33, further comprising a
15 register that is configurable to store the digital value and to provide the digital
16 value to the reference voltage driver, the register being readable and writable.
17

18 **38.** An integrated circuit as recited in claim 33, further comprising a
19 digitally controllable variable resistor that controls the gain of the reference
20 voltage driver.
21

22 **39.** An integrated circuit as recited in claim 33, wherein the feedback
23 receiver comprises a low-pass filter that does not significantly affect the input
24 characteristics of the feedback receiver.
25

1 **40.** An integrated circuit as recited in claim 33, wherein the distributed
2 reference voltage is routed similarly to the data and feedback receivers so that said
3 relative voltage change in the distributed reference voltage is approximately the
4 same at each of the data and feedback receivers.

5
6 **41.** An integrated circuit as recited in claim 33, wherein:
7 the distributed reference voltage is routed similarly to the data and feedback
8 receivers so that said relative voltage change in the distributed reference voltage is
9 approximately the same at each of the data and feedback receivers; and
10 the feedback receiver comprises a low-pass filter that does not significantly
11 affect the input characteristics of the feedback receiver.

12
13 **42.** An integrated circuit as recited in claim 33, wherein the integrated
14 circuit is a memory device that further comprises a plurality of memory storage
15 cells.

16
17 **43.** An integrated circuit, comprising:
18 receiver means for evaluating a plurality of data signals relative to a
19 distributed reference voltage;
20 feedback means for evaluating the distributed reference voltage relative to a
21 nominal reference voltage to produce a feedback signal;
22 driver means having a variable gain for producing a compensated reference
23 voltage;
24 routing means for routing the compensated reference voltage on the
25 integrated circuit to form the distributed reference voltage at the receiver and

1 feedback means, wherein the input characteristics of the receiver and feedback
2 means cause a voltage change in the distributed reference voltage at the receiver
3 and feedback means relative to the compensated reference voltage;

4 the receiver and feedback means having similar input characteristics so that
5 said relative voltage change in the distributed reference voltage is approximately
6 the same at each of the receiver and feedback means; and

7 gain control means for controlling the gain of the driver means in response
8 to the feedback signal so that the distributed reference voltage is approximately
9 equal to the nominal reference voltage.

10
11 **44.** An integrated circuit as recited in claim 43, wherein the gain control
12 means comprises a counter that produces a digital value, wherein the counter is
13 responsive to the feedback to increment and decrement the digital value.

14
15 **45.** An integrated circuit as recited in claim 43, wherein the gain control
16 means comprises a register that is configurable to store a digital value, the variable
17 gain of the driver means being responsive to the digital value.

18
19 **46.** An integrated circuit as recited in claim 43, wherein the gain control
20 means comprises a register that is configurable to store a digital value, the variable
21 gain of the driver means being responsive to the digital value, the register being
22 readable and writable.

1 **47.** An integrated circuit as recited in claim 43, wherein the
2 compensated reference voltage is distributed over impedance-matched conductors
3 to form the distributed reference voltage at the receiver and feedback means.

4
5 **48.** An integrated circuit as recited in claim 43, wherein the gain control
6 means is enabled during an initialization period to adjust the gain of the driver
7 means, wherein the gain control means is configured to maintain the gain of the
8 driver means constant during a subsequent operational period.

9
10 **49.** An integrated circuit as recited in claim 43, wherein the gain control
11 means comprises a digitally controllable variable resistor.

12
13 **50.** An integrated circuit as recited in claim 43, wherein the distributed
14 reference voltage is routed similarly to the receiver and feedback means so that
15 said relative voltage change in the distributed reference voltage is approximately
16 the same at each of the receiver and feedback means.

17
18 **51.** An integrated circuit as recited in claim 43, wherein:
19 wherein the distributed reference voltage is routed similarly to the receiver
20 and feedback means so that said relative voltage change in the distributed
21 reference voltage is approximately the same at each of the receiver and feedback
22 means; and

23 the feedback means comprises a low-pass filter that does not significantly
24 affect the input characteristics of the op-amp.
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1 52. An integrated circuit as recited in claim 43, wherein the integrated
2 circuit is a memory device that further comprises a plurality of memory storage
3 cells.

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5 53. A memory device comprising:
6 a plurality of memory storage cells;
7 a plurality of data receivers that evaluate binary data signals with reference
8 to a distributed reference voltage;

9 a feedback receiver that evaluates the distributed reference voltage relative
10 to a nominal reference voltage to produce a feedback signal;

11 a reference voltage driver that produces a compensated reference voltage,
12 the compensated reference voltage being routed on the memory device to form the
13 distributed reference voltage at the data and feedback receivers, wherein the input
14 characteristics of the data and feedback receivers cause a voltage change in the
15 distributed reference voltage at each receiver relative to the compensated reference
16 voltage;

17 the data and feedback receivers having similar input characteristics so that
18 said relative voltage change in the distributed reference voltage is approximately
19 the same at each of the data and feedback receivers; and

20 wherein the reference voltage driver has a variable gain that is configurable
21 to increase in response to the feedback signal when the distributed reference
22 voltage is less than the nominal reference voltage and to decrease in response to
23 the feedback signal when the distributed reference voltage is greater than the
24 nominal reference voltage.

1 **54.** A memory device as recited in claim 53, wherein the compensated
2 reference voltage is distributed over impedance-matched conductors to form the
3 distributed reference voltage at the data and feedback receivers.

4
5 **55.** A memory device as recited in claim 53, wherein the variable gain
6 of the reference voltage driver is controlled by a digital value, the integrated
7 circuit further comprising a register that is configurable to store the digital value
8 and to provide the digital value to the reference voltage driver.

9
10 **56.** A memory device as recited in claim 53, wherein the variable gain
11 of the reference voltage driver is controlled by a digital value, the integrated
12 circuit further comprising a register that is configurable to store the digital value
13 and to provide the digital value to the reference voltage driver, the register being
14 readable and writable.

15
16 **57.** A memory device as recited in claim 53, wherein the gain of the
17 reference voltage driver remains constant during an operational period that follows
18 an initialization period.

19
20 **58.** A memory device as recited in claim 53, wherein the feedback
21 receiver comprises a low-pass filter that does not significantly affect the input
22 characteristics of the feedback receiver.
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1 **59.** A memory device as recited in claim 53, wherein:
2 the distributed reference voltage is routed similarly to the data and feedback
3 receivers so that said relative voltage change in the distributed reference voltage is
4 approximately the same at each of the data and feedback receivers; and
5 the feedback receiver comprises a low-pass filter that does not significantly
6 affect the input characteristics of the feedback receiver.

7
8 **60.** A method comprising:
9 evaluating a plurality of signals relative to a distributed voltage;
10 amplifying a nominal voltage by a variable gain to produce a compensated
11 voltage;
12 routing the compensated reference voltage over resistive conductors to form
13 the distributed voltage;
14 increasing the variable gain when the distributed voltage is less than the
15 nominal voltage; and
16 decreasing the variable gain when the distributed voltage is greater than the
17 nominal voltage.

18
19 **61.** A method as recited in claim 60, wherein the routing comprises
20 routing the compensated reference voltage over impedance-matched resistive
21 conductors to form the distributed voltage.

22
23 **62.** A method as recited in claim 60, further comprising:
24 maintaining the variable gain at a constant value during an operational
25 period following an initialization period.